HOME | ABOUT | EXPERTISE | SOLUTIONS | GLOSSARY | CONTACT

ELECTRONIC MANUFACTURING SOLUTIONS

Glossary of Electronics Manufacturing Services (EMS) Acronyms

A | B | C | D | E | F | G | H | I | J | K | L | M
N | O | P | Q | R | S | T | U | V | W | X | Y | Z

For a PDF Version of this glossary click here to download. To view this download you will need Adobe Acrobat Reader (91k file)

ANSI American National Standards Institute

AOI Automated Optical Inspection. Test fixture method in which printed circuit boards are check at bare-board, pre- or post-soldered stages of assembly by optical means.

AML Approved Manufacturer List

ASIC Application Specific Integrated Circuit

ASTM American Society for Testing and Materials

ASQ American Society For Quality

ATE Automatic Test Equipment. Equipment designed to automatically analyze functional or static parameters in order to evaluate performance degradation. It may also be designed to perform fault

isolation.

ATG Automatic Test Generation. Computer generation of a test program based solely on the circuit technology, requiring little or no manual programming effort.

AVL Approved Vendor List

BGA Ball Grid Array. A component whose terminations are on the bottom of the package, and are in the shape of solder balls and in a grid array pattern. This generally covers components that have them in a full array or in a partial array with "missing" balls in the center.

Blackpad Poor solderability caused by contamination between the gold and nickel plating.

CAD Computer Aided Design. A computer based system to assist designers in the design, topological layout and drawing of an electronic component, assembly, or system.

CBGA/ CCGA	Ceramic Ball Grid Array/Ceramic Column Grid Array. A grid array packaged component that has ceramic as the substrate of the package, and may have either solder balls or solder columns for connections.
Convection Reflow	Soldering using forced hot air
CFC	Chlorinated Fluorocarbon; illegal to use.
CMOS	Complementary Metal Oxide Semiconductor
COB	Chip-on-Board. A situation where the silicon IC chip is mounted directly to the electronic assembly substrate or PWB without an intermediate packaging step. Connections between the chip and the board are generally made with bond wired (also sometime called chip and wire), but the terminology is occasionally used for any chip connection technique such as flip chip (solderable bumps or tape automated bonding).
C of C	Certificate of Compliance
CSP	Chip Scale Package. Active, multi-I/O package that is no larger than 125% of the size of the silicon IC.

CTE	Coefficient of Thermal Expansion. See TCE
DFM	Design for Manufacturability
DFT	Design for Test
DI	De-Ionized water
DIP	Dual In-Line Package. A popular through hole package with leads in rows on opposite sides of the package.
DPM	Defects Per Million
DPMO	Defects Per Million Opportunities
DRAM	Dynamic RAM. Read-write memory that must be refreshed (read or written into) periodically to maintain the storage of information.
DUT	Device Under Test. Component, PCB, or assembly subjected to a test. Also known as unit under test (UTT) and loaded board.
EIA	Electronic Industries Alliance
EGIN	Electroless Gold over Immersion Nickel
ESD	Electrostatic Discharge. A transfer of electrostatic charge between bodies at different electrostatic potentials caused by direct contact or induced by an electrostatic field.

ESS	Environmental Stress Screening. Manufacturing stage in which all assemblies are subjected to thermal stresses, with the aim of forcing all early failures to occur. Also known as reliability testing.
Eutectic	Solder that have a very short transition from liquid to solid, an optimal mix with no plastic state
FPT	Fine Pitch Technology. The portion of surface mount technology that included components that typically have lead pitch, or center-to-center spacing, between 0.4mm and 0.8mm.
FP	Flat Pack. A low profile IC package, which typically has gull wing type of leads on two or four sides.
FR-4	The most commonly used epoxy-fiberglass material standard for printed circuit boards. The "FR" refers to flame retardant.
HASL	Hot Air Soldered Leveled. Hot air is used to blow off the excess after the TWS is dipped in solder. Typically used to the SMOBC process.

IC	Integrated Circuit. A small, complete circuit made by vacuum deposition and other techniques, usually on a silicon chip, and mounted in a package.
IEEE	Institute of Electrical and Electronics Engineers
IMAPS	International Microelectronics and Packaging Society
IMB	Intermetallic Bond, thin layer of chemical bonding in metals - see IMC
IMC	Intermetallic Compound. Metallic compounds that form at the interfaces between different metals, such as copper-tin compounds that form at the interface of a solder joint and a copper lead. IMCs typically have significantly different properties, such as tensile strength.
IPC	Institute for Interconnecting and Packaging Electronic Circuits Class 1,2,3 class under IPC quality - class 1 is general electronics (disposable), class 2 is dedicated service electronics (repairable), class 3 is high performance electronics(high reliability).

IR	InfraRed. Soldering process that uses infrared energy as the primary method of heating.
ISO	International Standards Organization
JEDEC	Joint Electronic Devices Engineering Council, a part of the Electronic Industries Association (EIA) that publishes specifications and standards for electronic components.
KGB	Known Good Board. A correctly operating PCB. It is used in learning or debugging a test program in development and for comparison testers where it serves as the standard unit by which other PCBs are compared.
KGD	Known Good Die
LCCC	Leadless Ceramic Chip Carrier. A hermetically sealed ceramic package that has pads (castellations) around its sides for solder connection in a surface mounting application.
LCC	See LCCC
LGA	Leadless Gate Array

LSI	Large Scale Integration. Arrays of ICs on a single substrate that comprise 100 or more individual active circuit functions or gates.
MCM	Multichip Module. A circuit comprised of two or more silicon devices bonded directly to a substrate by wire bond, TAB or flip chip.
MELF	Metal Electrode Face Bonding. A cylindrical leadless component with a round body and metals terminals on the ends.
MLF	Micro Lead Frame
MSD	Moisture Sensitive Device
MTBF	Mean Time Between Failures. The arithmetic or statistical mean average time interval, usually in hours, that may be expected between failures of an operating unit. Results should be designated actual, predicted, or calculated.
Nodules	Metal debris in plated through holes that is plated over
OA	Organic aqueous, water soluble flux

OSP — Organic Solder Preservative. Layers of organic coatings applied to entire boar surfaces to prevent oxidation and to retain solderability.

PBGA — Plastic Ball Grid Array. A ball grid array component whose package substrate is made of plastic, most likely an FR-4 equivalent of epoxy-fiberglass, polyimidearramid, or similar resin-fiber combinations.

PCA — Printed Circuit Assembly. The generic term for a PCB after all electrical components have been attached. Also referred to as a printed wiring assembly (PWA).

PCB — [illegible] manufactured from a rigid base material upon which a completely processed printed circuit has been formed.

PGA — Pin Grid Array. Similar to a pin grid array. An IC package that has solderable connections in a grid layout on the bottom of the package, and is soldered to the surface of the substrate (PWB) with butt solder joints.

PCMCIA	Personal Computer Memory Card International Association. The organization that has developed the early standards for the various sizes of modules which were initially for memory expansion but are now used for many different electronic functions.
PLCC	Plastic Leaded Chip Carrier. A plastic IC package for surface mounting applications that has leads, generally "J" leads, on all four sides.
PPM	Parts Per Million
PQFN	Plastic Quad Flatpack with no leads,Leadless CSP components.
PQFP	Plastic Quad Flat Pack. An FP with leads on four sides generally refers to a plastic quad flat package that is built to SEDEC standards.
PTH	Plated Through Hole. An interconnection from one side of a PWB (PCB) to another that is formed with the plating of the hole sidewalls.

PWA	Printed Wiring Board. The substrate, generally epoxy glass, used to provide component attachment lands and interconnections to form a functioning electronic circuit (also called a PCB or printed circuit board).
PWB	Printed Wiring Assembly. The generic term for a PWB after all electrical components have been attached.
QFP	Quad Flat Pack. A FP with leads on four sides. Generally refers to a plastic quad flat package that is built to SEDEC standards.
QSOP	Quarter-Size Small Outline Package. An SO style IC package that has leads on a 25 mil pitch. The name derives from the fact that the package is approximately _ the length and _ the width of a standard SOIC, and thus a package of the same pin count occupies approximately _ the area on a PWB.
RAM	Random Access Memory. A type of memory that offers access to storage locations within it by means of X and Y coordinates.

Reflow	The melting of solder paste into solder, typically in a in-line oven
ROM	Read Only Memory. A random access storage in which the data pattern is unchangeable after manufacture.
SEM	Scanning Electron Microscope
SIP	Single-In-Line Package. An IC package or multi-component sub-assembly that has connections or leads in a single row on one side.
SIR	Surface Insulation Resistance
Slivers	Thin pieces of metal from a machining process
SMA	Surface Mount Assembly. An electronic assembly or module that is manufactured with surface mounted components and suing surface mount technology.
SME	Society of Manufacturing Engineers
SMTA	Surface Mount Technology Association
SMD	Surface mount device. Any electrical or mechanical device that can be attached to the surface of a substrate with solder.

SMOBC	Solder Mask Over Bare Copper. A printed wiring board manufacturing technique whereby solder mask is applied over bare copper, exposed and developed, and then the board is dipped in molten solder to coat the exposed copper.
SMT	Surface Mount Technology. The technology used to manufacture electronic assemblies using com0ponents that are soldered directly to the surface of the substrate or PWB.
SO	Small Outline. A package resembling a flat pack with leads on only two sides.
SOIC	Small Outline Integrated Circuit. A plastic IC package for surface mounting applications that has leads on two opposites sides.
SOJ	A plastic IC package with “J” leads on two sides. It resembles a plastic DIP or a SOIC except for lead spacing and forming.
SOL/SOW	Small Outline-Large/Small Outline Wide. SO generally refers to a package that is approximately 150 mils wide, while SOL/SOW refers to packages that are approximately 300 mils wide.

SOP	VSOP/SSOP. Another designation for the small outline ICP packages, i.e. Small Outline Package (Very Small Outline Package, Shrink Small Outline Package).
SOT	Small Outline Transistor. A plastic leaded package for diodes and transistors used in surface mounting applications.
SPC	Statistical Process Control. The use of statistical techniques to analyze a process or its output to determine any variation from a benchmark and to take appropriate action to restore statistical control, if required.
SSOIC	Shrink Small Outline IC. An SO style IC package that has leads on a 25 mil pitch.
TAB	Tape Automated Bonding. An IC interconnection process that uses organic tape to support pre-formed leads during bonding to the chip (inner lead bonding-ILB) and connection to the substrate (outer lead bonding-OLB). The IC chip is usually bare during the interconnecting processes.

TBGA	Tape Ball Grid Array. A ball grid array component package that uses TAB techniques to make the connections between the IC chip and the solder balls. This results in a solder ball grid array that is only around the periphery, and leaves compliant connections between the IC and the solder balls for better TCE reliability.
TCE	(CTE) Thermal Coefficient of Expansion (Coefficient of Thermal Expansion). The rate of expansion (ppm/C) of a material when its temperature is increased.
Telcordia	Formerly Bellcore, telecommunication (telephone) industry standards
UBGA	micro BGA .8mm ball spacing of less
VFP	Very Fine Pitch. The center-to-center lead distance of surface mount packages that are between 0.012 inch and 0.020 inch.
VLSI	Very Large Scale Integration
VSOIC	Very Small Outline IC. A SO style IC package that has leads with a pitch of 30 mils or less.
WIP	Work In Progress

Wiskers	Tin or silver growths of metal in thin strands

Glossary compiled and provided by AQS, Inc.

AQS, INC • 3040 N. FIRST STREET • SAN JOSE, CA 95134 • P: 408.432.8300 • F: 408.432.6090

© 2004 AQS, Inc - All rights reserved